8XC251SA/SB/SP/SQ
HIGH-PERFORMANCE CHMOS MICROCONTROLLER

Commercial/Express

- Real Time and Programmed Wait State Bus Operation
- Binary-code Compatible with MCS® 51
- Pin Compatible with 44-lead PLCC and 40-lead PDIP MCS 51 Sockets
- Register-based MCS® 251 Architecture
  - 40-byte Register File
  - Registers Accessible as Bytes, Words, and Double Words
- Enriched MCS 51 Instruction Set
  - 16-bit and 32-bit Arithmetic and Logic Instructions
  - Compare and Conditional Jump Instructions
  - Expanded Set of Move Instructions
- Linear Addressing
- 256-Kbyte Expanded External Code/Data Memory Space
- ROM/OTPROM/EPROM Options: 16 Kbytes (SB/SQ), 8 Kbytes (SA/SP), or without ROM/OTPROM/EPROM
- 16-bit Internal Code Fetch
- 64-Kbyte Extended Stack Space
- On-chip Data RAM Options: 1-Kbyte (SA/SB) or 512-Byte (SP/SQ)
- 8-bit, “Min” 2-clock External Code Fetch in Page Mode
- User-selectable Configurations:
  - External Wait States (0-3 wait states)
  - Address Range & Memory Mapping
  - Page Mode
- 32 Programmable I/O Lines
- Seven Maskable Interrupt Sources with Four Programmable Priority Levels
- Three Flexible 16-bit Timer/counters
- Hardware Watchdog Timer
- Programmable Counter Array
  - High-speed Output
  - Compare/Capture Operation
  - Pulse Width Modulator
  - Watchdog Timer
- Programmable Serial I/O Port
  - Framing Error Detection
  - Automatic Address Recognition
- High-performance CHMOS Technology
- Static Standby to 16-MHz Operation
- Complete System Development Support
  - Compatible with Existing Tools
  - New MCS 251 Tools Available: Compiler, Assembler, Debugger, ICE
- Package Options (PDIP, PLCC, and Ceramic DIP)
- Fast MCS 251 Instruction Pipeline

This document contains information on products with “[M] [C] '94 '95 C” as the last line of the top marking diagram. A member of the Intel family of 8-bit MCS 251 microcontrollers, the 8XC251SA/SB/SP/SQ is binary-code compatible with MCS 51 microcontrollers and pin compatible with 40-lead PDIP and 44-lead PLCC MCS 51 microcontrollers. MCS 251 microcontrollers feature an enriched instruction set, linear addressing, and efficient C-language support. The 8XC251SA/SB/SP/SQ has 512 bytes or 1 Kbyte of on-chip RAM and is available with 8 Kbytes or 16 Kbytes of on-chip ROM/OTPROM/EPROM, or without ROM/OTPROM/EPROM. A variety of features can be selected by new user-programmable configurations.

July 2004 **Order Number:** 272783-004

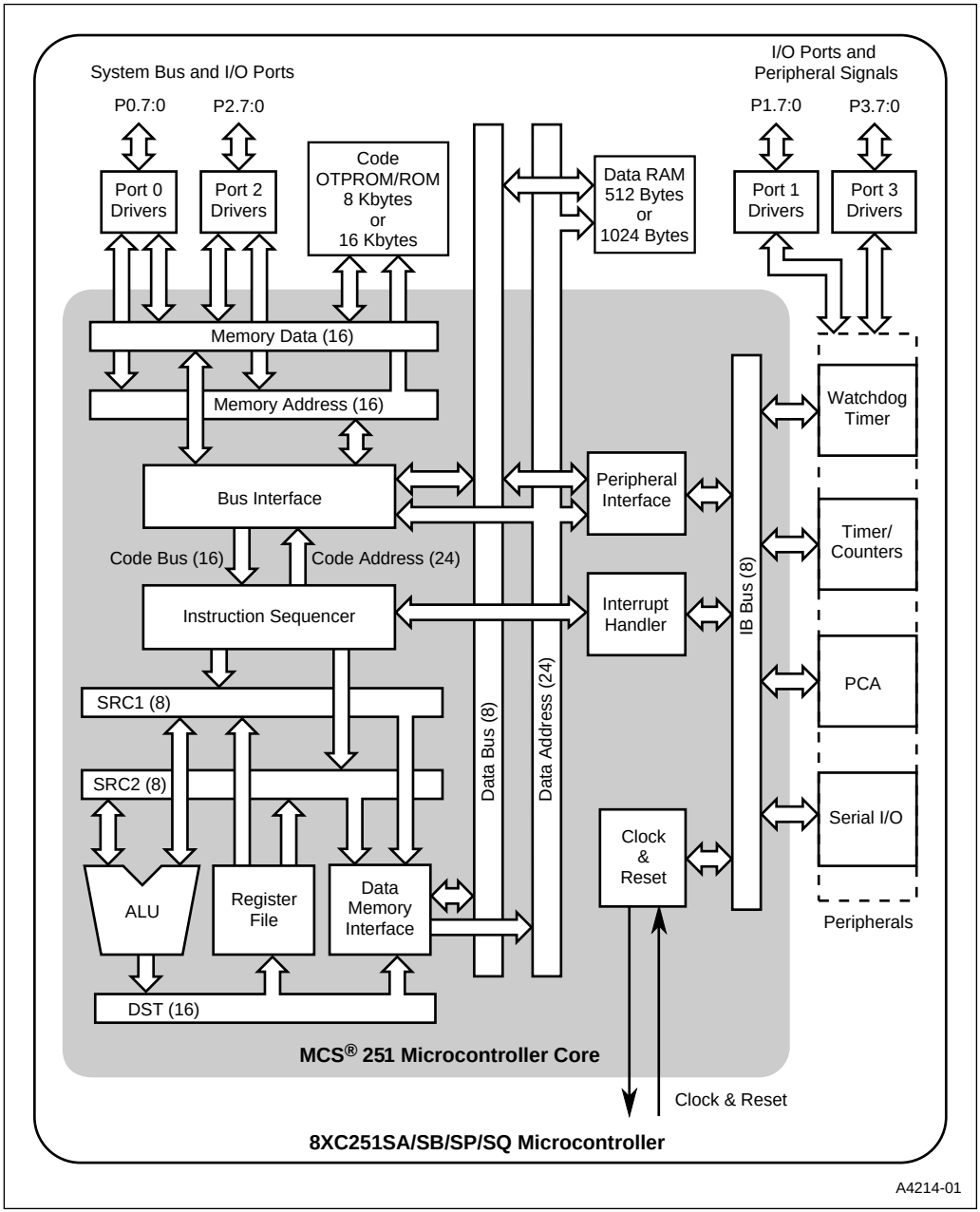


Figure 1. 8XC251SA/SB/SP/SQ Block Diagram

TEMPERATURE RANGE

With the commercial (standard) temperature option, the device operates over the temperature range 0°C to +70°C. The express temperature option provides -40°C to +85°C device operation.

PROLIFERATION OPTIONS

Table 1 lists the proliferation options. See Figure 2 for the 8XC251SA/SB/SP/SQ family nomenclature.

Table 1. Proliferation Options

8XC251SA/SB/SP/SQ (0 – 16 MHz; 5 V ±10%)	
80C251SB16	CPU-only
80C251SQ16	CPU-only
83C251SA16	ROM
83C251SB16	ROM
83C251SP16	ROM
83C251SQ16	ROM
87C251SA16	OTPROM/EPROM
87C251SB16	OTPROM/EPROM
87C251SP16	OTPROM/EPROM
87C251SQ16	OTPROM/EPROM

PROCESS INFORMATION

This device is manufactured on a complimentary high-performance metal-oxide semiconductor (CHMOS) process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook* (order number 210997).

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values change depending on operating conditions and application requirements. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology.

Table 2. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
44-lead PLCC	46°C/W	16°C/W
40-lead PDIP	45°C/W	16°C/W
40-lead Ceramic DIP	30.5°C/W	10°C/W

PACKAGE OPTIONS

Table 3 lists the 8XC251SA/SB/SP/SQ packages.

Table 3. Package Information

Pkg.	Definition	Temperature
X	44 ld. PLCC	0°C to +70°C
X	40 ld. Plastic DIP	0°C to +70°C
X	40 ld. Ceramic DIP	0°C to +70°C
X	44 ld. PLCC	-40°C to +85°C
X	40 ld. Plastic DIP	-40°C to +85°C

NOTE: To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".

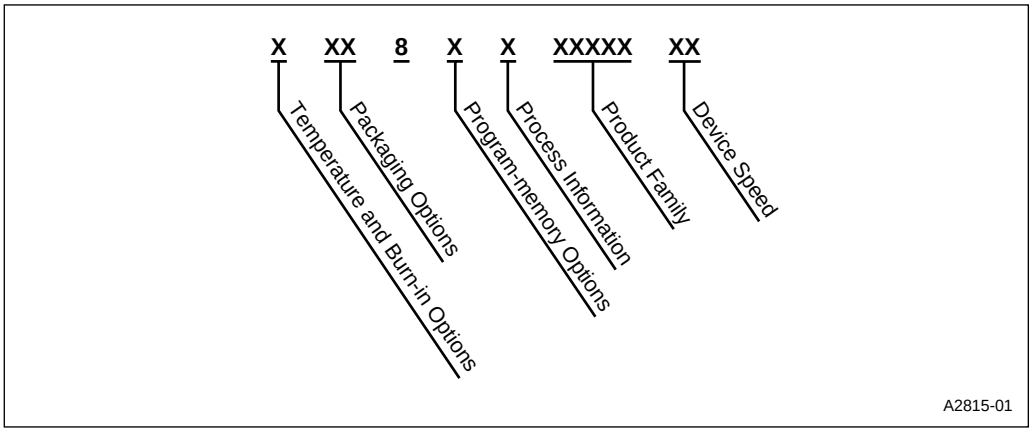


Figure 2. The 8XC251SA/SB/SP/SQ Family Nomenclature

Table 4. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
	X	Express operating temperature range (-40°C to 85°C) with Intel standard burn-in.
Packaging Options	X	44-lead Plastic Leaded Chip Carrier (PLCC)
	X	40-lead Plastic Dual In-line Package (PDIP)
	X	40-lead Ceramic Dual In-line Package (Ceramic DIP)
Program Memory Options	0	Without ROM/OTPROM/EPROM
	3	ROM
	7	User programmable OTPROM/EPROM
Process Information	C	CHMOS
Product Family	251	8-bit control architecture
Device Memory Options	SA	1-Kbyte RAM/8-Kbyte ROM/OTPROM/EPROM
	SB	1-Kbyte RAM/16-Kbyte ROM/OTPROM/EPROM or without ROM/OTPROM/EPROM
	SP	512-byte RAM/8-Kbyte ROM/OTPROM/EPROM
	SQ	512-byte RAM/16-Kbyte ROM/OTPROM/EPROM or without ROM/OTPROM/EPROM
Device Speed	16	External clock frequency

NOTES:
1. To address the fact that many of the package prefix variables have changed, all package prefix variables in the document are now indicated with an "**x**".

Table 5. 8XC251SA/SB/SP/SQ Memory Map

Internal Address)	Description	Notes
FF:FFFFH FF:4000H	External Memory (FF:FFF8H–FF:FFFFH are internally decoded for Configuration Byte data in all ROM/OTPROM/EPROM devices with EA# = 1. For all devices with EA# = 0, the last 8 bytes of the external address range FF:XFF8H–FF:XFFFH contain Configuration Byte information).	1, 3, 10
FF:3FFFH FF:0000H	External memory or for internal ROM/OTPROM/EPROM devices: 16-Kbytes of internal addresses as determined by the EA# pin (Table 8). Note: 8-Kbyte internal ROM/OTPROM/EPROM array addresses end at FF:1FFFH.	3, 4, 5
FE:FFFFH FE:0000H	External Memory	3
FD:FFFFH FD:0000H	Reserved	6
FC:FFFFH FC:0000H	Reserved	6
FB:FFFFH 04:0000H	Reserved	6
03:FFFFH 03:0000H	Reserved	6
02:FFFFH 02:0000H	Reserved	6
01:FFFFH 01:0000H	External Memory	3
00:FFFFH 00:E000H	External memory or with EMAP# bit = 0 this address range for 16-Kbyte devices is redirected to internal ROM/OTPROM/EPROM array region.	5, 7
00:DFFFH 00:0420H	External Memory	7
00:041FH 00:0080H	On-chip RAM (512 byte RAM devices end at 00:021FH	7
00:007FH 00:0020H	On-chip RAM	8
00:001FH 00:0000H	Storage for R0–R7 of Register File	2, 9

NOTES:
1. 18 address lines are bonded out (A15:0, A16:0, or A17:0 selected during chip configuration).
2. The special function registers (SFRs) and the register file have separate internal address spaces.
3. Data in this area is accessible by indirect addressing only.
4. Devices can reset into different internal or external starting locations depending on the state of EA# and configuration register information (see EA#. See also UCONFIG1:0 bit definitions).
5. The 16-Kbyte ROM/OTPROM/EPROM devices allow internal locations FF:2000H–FF:3FFFH to map into region 00:. In this case, if EA# = 1, a data read to 00:E000H–00:FFFFH is redirected to internal ROM/OTPROM/EPROM (see bit 1 in UCONFIG0). This is not available for 8-Kbyte ROM/OTPROM/EPROM devices.
6. This reserved area returns unspecified values and writes no data.
7. Data is accessible by direct and indirect addressing.
8. Data is accessible by direct, indirect, and bit addressing.
9. Data is accessible by direct, indirect, and register addressing.
10. Eight addresses at the top of all external memory maps are reserved for current and future device configuration byte information.

8XC251SA/SB/SP/SQ 44-lead PLCC Package

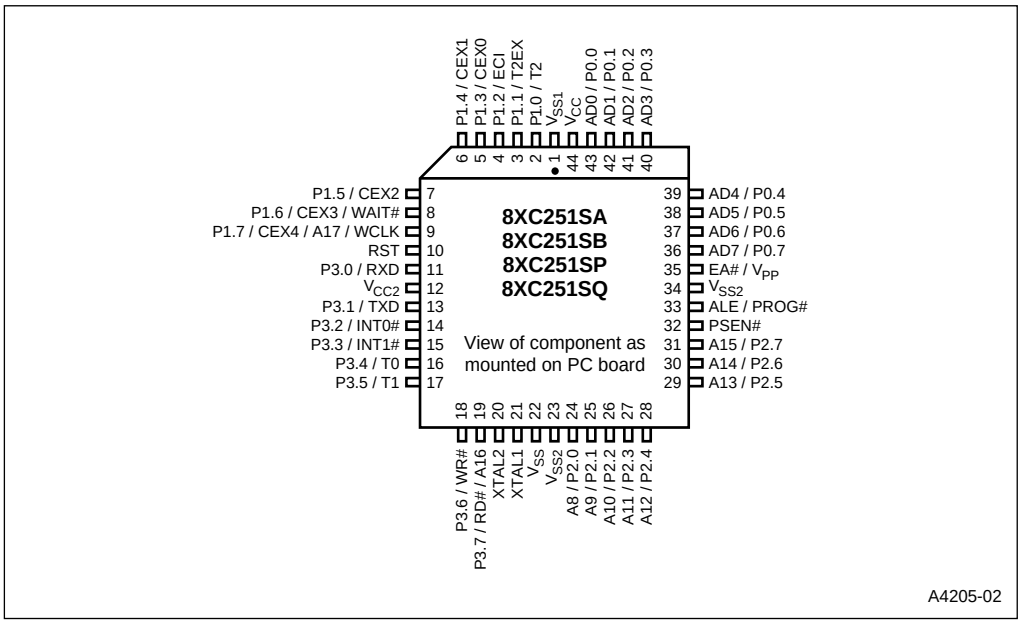


Figure 3. 8XC251SA/SB/SP/SQ 44-lead PLCC Package

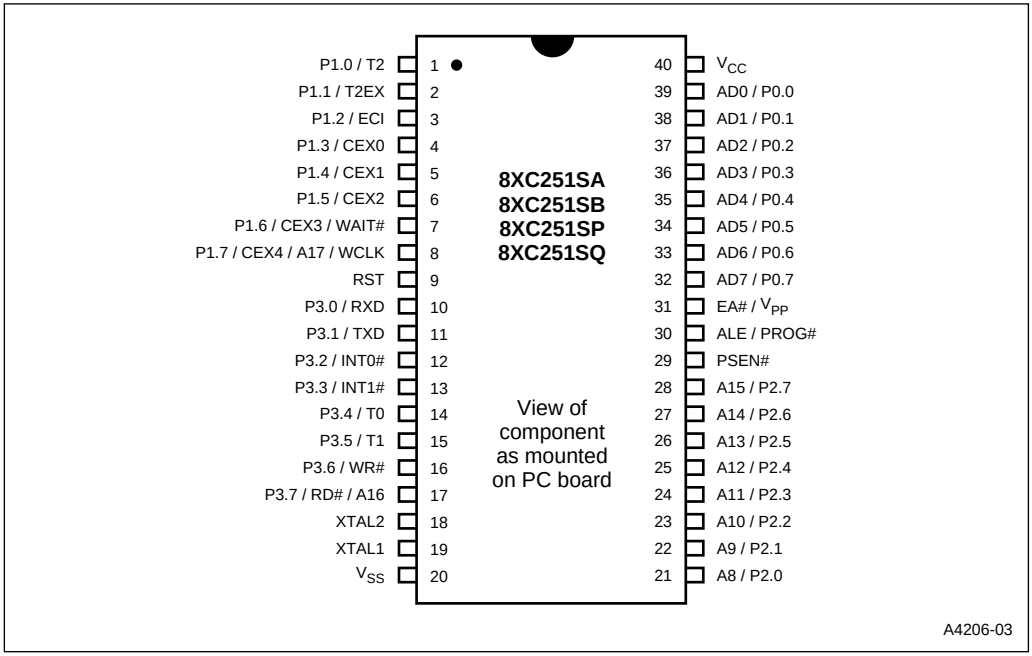


Figure 4. 8XC251SA/SB/SP/SQ 40-lead PDIP and Ceramic DIP Packages

Table 6. PLCC/DIP Lead Assignments Listed by Functional Category

Address & Data		
Name	**PLCC**	**DIP**
AD0/P0.0	43	39
AD1/P0.1	42	38
AD2/P0.2	41	37
AD3/P0.3	40	36
AD4/P0.4	39	35
AD5/P0.5	38	34
AD6/P0.6	37	33
AD7/P0.7	36	32
A8/P2.0	24	21
A9/P2.1	25	22
A10/P2.2	26	23
A11/P2.3	27	24
A12/P2.4	28	25
A13/P2.5	29	26
A14/P2.6	30	27
A15/P2.7	31	28
P3.7/RD#/A16	19	17
P1.7/CEX4/A17/WCLK	9	8

Processor Control		
Name	**PLCC**	**DIP**
P3.2/INT0#	14	12
P3.3/INT1#	15	13
EA#/V_{PP}	35	31
RST	10	9
XTAL1	21	18
XTAL2	20	19

Input/Output		
Name	**PLCC**	**DIP**
P1.0/T2	2	1
P1.1/T2EX	3	2
P1.2/ECI	4	3
P1.3/CEX0	5	4
P1.4/CEX1	6	5
P1.5/CEX2	7	6
P1.6/CEX3/WAIT#	8	7
P1.7/CEX4/A17/WCLK	9	8
P3.0/RXD	11	10
P3.1/TXD	13	11
P3.4/T0	16	14
P3.5/T1	17	15

Power & Ground		
Name	**PLCC**	**DIP**
V_{CC}	44	40
V_{CC2}	12	
V_{SS}	22	20
V_{SS1}	1	
V_{SS2}	23, 34	
EA#/V_{PP}	35	31

Bus Control & Status		
Name	**PLCC**	**DIP**
P3.6/WR#	18	16
P3.7/RD#/A16	19	17
ALE/PROG#	33	30
PSEN#	32	29

Table 7. Lead Assignments Arranged by Lead Number

PLCC	DIP	Name
1		V_{SS1}
2	1	P1.0/T2
3	2	P1.1/T2EX
4	3	P1.2/ECI
5	4	P1.3/CEX0
6	5	P1.4/CEX1
7	6	P1.5/CEX2
8	7	P1.6/CEX3/WAIT#
9	8	P1.7/CEX4/A17/WCLK
10	9	RST
11	10	P3.0/RXD
12		V_{CC2}
13	11	P3.1/TXD
14	12	P3.2/INT0#
15	13	P3.3/INT1#
16	14	P3.4/T0
17	15	P3.5/T1
18	16	P3.6/WR#
19	17	P3.7/RD#/A16
20	18	XTAL2
21	19	XTAL1
22	20	V_{SS}

PLCC	DIP	Name
23		V_{SS2}
24	21	A8/P2.0
25	22	A9/P2.1
26	23	A10/P2.2
27	24	A11/P2.3
28	25	A12/P2.4
29	26	A13/P2.5
30	27	A14/P2.6
31	28	A15/P2.7
32	29	PSEN#
33	30	ALE/PROG#
34		V_{SS2}
35	31	EA#/V_{PP}
36	32	AD7/P0.7
37	33	AD6/P0.6
38	34	AD5/P0.5
39	35	AD4/P0.4
40	36	AD3/P0.3
41	37	AD2/P0.2
42	38	AD1/P0.1
43	39	AD0/P0.0
44	40	V_{CC}

SIGNAL DESCRIPTIONS

Table 8. Signal Descriptions

Signal Name	Type	Description	Alternate Function
A17	O	**18th Address Bit (A17).** Output to memory as 18th external address bit (A17) in extended bus applications, depending on the values of bits RD0 and RD1 in configuration byte UCONFIG0 (see Table 9). See also RD# and PSEN#.	P1.7/CEX4/ WCLK
A16	O	**Address Line 16**. See RD#.	RD#
A15:8†	O	**Address Lines**. Upper address lines for the external bus.	P2.7:0
AD7:0†	I/O	**Address/Data Lines**. Multiplexed lower address lines and data lines for external memory.	P0.7:0
ALE	O	**Address Latch Enable**. ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. An external latch can use ALE to demultiplex the address from the address/data bus.	PROG#
CEX4:0	I/O	**Programmable Counter Array (PCA) Input/Output Pins**. These are input signals for the PCA capture mode and output signals for the PCA compare mode and PCA PWM mode.	P1.6:3 P1.7/A17/ WAIT#
EA#	I	**External Access**. Directs program memory accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off-chip. For EA# = 1, an access is to on-chip ROM/OTPROM/EPROM if the address is within the range of the on-chip ROM/OTPROM/EPROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without on-chip ROM/OTPROM/EPROM, EA# must be strapped to ground.	V_{PP}
ECI	I	**PCA External Clock Input**. External clock input to the 16-bit PCA timer.	P1.2
INT1:0#	I	**External Interrupts 0 and 1**. These inputs set bits IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits INT1:0 are clear, bits IE1:0 are set by a low level on INT1:0#.	P3.3:2
PROG#	I	**Programming Pulse**. The programming pulse is applied to this pin for programming the on-chip OTPROM.	ALE
P0.7:0	I/O	**Port 0**. This is an 8-bit, open-drain, bidirectional I/O port.	AD7:0
P1.0 P1.1 P1.2 P1.7:3	I/O	**Port 1**. This is an 8-bit, bidirectional I/O port with internal pullups.	T2 T2EX ECI CEX3:0 CEX4/A17/ /WAIT#/ WCLK
P2.7:0	I/O	**Port 2**. This is an 8-bit, bidirectional I/O port with internal pullups.	A15:8

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC and 40-lead DIP MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 8. Signal Descriptions (Continued)

Signal Name	Type	Description	Alternate Function
P3.0 P3.1 P3.3:2 P3.5:4 P3.6 P3.7	I/O	**Port 3**. This is an 8-bit, bidirectional I/O port with internal pullups.	RXD TXD INT1:0# T1:0 WR# RD#/A16
PSEN#	O	**Program Store Enable**. Read signal output. This output is asserted for a memory address range that depends on bits RD0 and RD1 in configuration byte UCONFIG0 (see RD# and Table 9):	—
RD#	O	**Read or 17th Address Bit (A16).** Read signal output to external data memory or 17th external address bit (A16), depending on the values of bits RD0 and RD1 in configuration byte UCONFIG0. (See PSEN# and):	P3.7/A16
RST	I	**Reset**. Reset input to the chip. Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pulldown resistor, which allows the device to be reset by connecting a capacitor between this pin and V_{CC}. Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation.	—
RXD	I/O	**Receive Serial Data**. RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2, and 3.	P3.0
T1:0	I	**Timer 1:0 External Clock Inputs**. When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count.	P3.5:4
T2	I/O	**Timer 2 Clock Input/Output**. For the timer 2 capture mode, this signal is the external clock input. For the clock-out mode, it is the timer 2 clock output.	P1.0
T2EX	I	**Timer 2 External Input**. In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 registers to be reloaded. In the up-down counter mode, this signal determines count direction: 1=up, 0=down.	P1.1
TXD	O	**Transmit Serial Data**. TXD outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2, and 3.	P3.1
V_{CC}	PWR	**Supply Voltage**. Connect this pin to the +5V supply voltage.	—
V_{CC2}	PWR	**Secondary Supply Voltage 2.** This supply voltage connection is provided to reduce power supply noise. Connection of this pin to the +5V supply voltage is recommended. However, when using the 8XC251SB as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility. (Not available on DIP)	—
V_{PP}	I	**Programming Supply Voltage**. The programming supply voltage is applied to this pin for programming the on-chip OTPROM/EPROM.	EA#
V_{SS}	GND	**Circuit Ground**. Connect this pin to ground.	—

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC and 40-lead DIP MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 8. Signal Descriptions (Continued)

Signal Name	Type	Description	Alternate Function
V_{SS1}	GND	**Secondary Ground**. This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8XC251SA/SB/SP/SQ as a pin-for-pin replacement for the 8XC51BH, V_{SS1} can be unconnected without loss of compatibility. (Not available on DIP)	—
V_{SS2}	GND	**Secondary Ground 2**. This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8XC251SB as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility. (Not available on DIP)	—
WAIT#	I	**Real Time Wait State Input.** The real time WAIT# input is enabled by writing a logical '1' to the WCON.0 (RTWE) bit at S:A7H. During bus cycles, the external memory system can signal 'system ready' to the microcontroller in real time by controlling the WAIT# input signal on the port 1.6 input.	P1.6/CEX3
WCLK	O	**Wait Clock Output.** The real time WCLK output is driven at port 1.7 (WCLK) by writing a logical '1' to the WCON.1 (RTWCE) bit at S:A7H. When enabled, the WCLK output produces a square wave signal with a period of one-half the ocillator frequency.	P1.7/CEX4/ A17
WR#	O	**Write**. Write signal output to external memory.	P3.6
XTAL1	I	**Input to the On-chip, Inverting, Oscillator Amplifier**. To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing.	—
XTAL2	O	**Output of the On-chip, Inverting, Oscillator Amplifier**. To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	—

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC and 40-lead DIP MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 9. Memory Signal Selections (RD1:0)

RD1:0	P1.7/CEX/ A17	RD#	PSEN#	WR#	Features
0 0	A17	RD# = A16	Asserted for all addresses	Asserted for writes to all memory locations	256-Kbyte external memory
0 1	P1.7/CEX4	RD# = A16	Asserted for all addresses	Asserted for writes to all memory locations	128-Kbyte external memory
1 0	P1.7/CEX4	P3.7 only	Asserted for all addresses	Asserted for writes to all memory locations	One additional port pin
1 1	P1.7/CEX4	Asserted for ≤ 7F:FFFFH	Asserted for ≥ 80:0000H	Asserted for all compatible MCS 51 memory locations	Compatible with MCS 51 microcontrollers

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature under Bias:
- Commercial ..... 0°C to +70°C
- Express ..... -40°C to +85°C

Storage Temperature ..... -65°C to +150°C
Voltage on EA#/V_{PP} Pin to V_{SS} ..... 0 V to +13.0 V
Voltage on Any other Pin to V_{SS} ..... -0.5 V to +6.5 V
I_{OL} per I/O Pin ..... 15 mA
Power Dissipation ..... 1.5 W

NOTE:

Maximum power dissipation is based on package heat-transfer limitations, not device power consumption.

OPERATING CONDITIONS†

T_A (Ambient Temperature Under Bias):
- Commercial ..... 0°C to +70°C
- Express ..... -40°C to +85°C

V_{CC} (Digital Supply Voltage) ..... 4.5 V to 5.5 V
V_{SS} ..... 0 V

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales Office that you have the latest datasheet before finalizing a design.

†***WARNING:*** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. Characteristics

Parameter values apply to all devices unless otherwise indicated.

Table 10. DC Characteristics at V_{CC} = 4.5 – 5.5 V

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#)	-0.5		$0.2V_{CC} - 0.1$	V	
V_{IL1}	Input Low Voltage (EA#)	0		$0.2V_{CC} - 0.3$	V	
V_{IH}	Input High Voltage (except XTAL1, RST)	$0.2V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	$0.7V_{CC}$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage (Port 1, 2, 3)			0.3 0.45 1.0	V	I_{OL} = 100 µA I_{OL} = 1.6 mA I_{OL} = 3.5 mA (Note 1, Note 2)
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)			0.3 0.45 1.0	V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA (Note 1, Note 2)
V_{OH}	Output High Voltage (Port 1, 2, 3, ALE, PSEN#)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA (Note 3)

NOTES:

1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10 mA

   Maximum I_{OL} per 8-bit port:
   port 0 26 mA
   ports 1–3 15 mA

   Maximum Total I_{OL} for all output pins 71 mA

   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{CC} = 5.0, T_A = 25°C and are not guaranteed.

Table 10. DC Characteristics at V_{CC} = 4.5 – 5.5 V (Continued)

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{OH1}	Output High Voltage (Port 0 in External Address)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
V_{oh2}	Output High Voltage (Port 2 in External Address during Page Mode)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
I_{IL}	Logical 0 Input Current (Port 1, 2, 3)			-50	µA	VIN = 0.45 V
I_{LI}	Input Leakage Current (Port 0)			+/-10	µA	0.45 < VIN < V_{CC}
I_{TL}	Logical 1-to-0 Transition Current (Port 1, 2, 3)			-650	µA	VIN = 2.0 V
R_{rst}	RST Pulldown Resistor	40		225	kΩ	
C_{io}	Pin Capacitance		10 (Note 4)		pF	F_{OSC} = 16 MHz T_A = 25 °C
I_{pd}	Powerdown Current		10 (Note 4)	< 20	µA	
I_{dl}	Idle Mode Current		5 (Note 4)	7	mA	F_{OSC} = 16 MHz
I_{CC}	Operating Current		20 (Note 4)	45	mA	F_{OSC} = 16 MHz

NOTES:

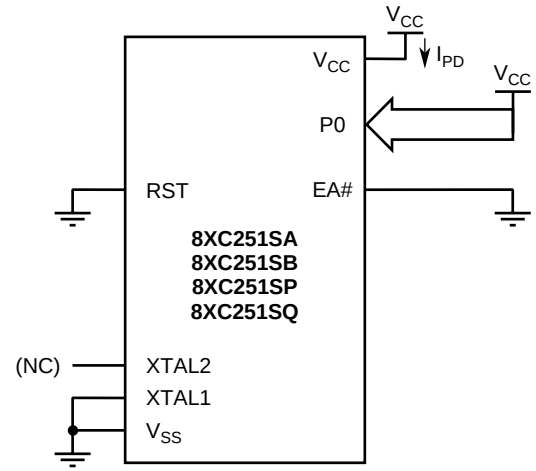
1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10 mA

   Maximum I_{OL} per 8-bit port:
   - port 0: 26 mA
   - ports 1–3: 15 mA

   Maximum Total I_{OL} for all output pins: 71 mA

   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{CC} = 5.0, T_A = 25°C and are not guaranteed.



All other 8XC251SA/SB/SP/SQ pins are unconnected.

A4208-01

Figure 5. I_{PD} Test Condition, Powerdown Mode, V_{CC} = 2.0 – 5.5V

A.C. Characteristics

Table 11 lists AC timing parameters for the 8XC251SA/SB/SP/SQ with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and/or by extending ALE. In the table, Notes 3 and 5 mark parameters affected by an ALE wait state, and Notes 4 and 5 mark parameters affected by a PSEN#/RD#/WR# wait state.

Figures 6–11 show the bus cycles with the timing parameters.

Table 11. AC Characteristics (Capacitive Loading = 50 pF)

Symbol	Parameter	@ Max F_{osc} (1)		F_{osc} Variable		Units
		Min	Max	Min	Max	
F_{OSC}	XTAL1 Frequency	N/A	N/A	0	16	MHz
T_{osc}	$1/F_{OSC}$ @ 12 MHz @ 16 MHz	N/A	N/A	 83.3 62.5		ns
T_{lhll}	ALE Pulse Width @ 12 MHz @ 16 MHz	 73.3 52.5		 (1+2M) T_{OSC} – 10		ns (3)
T_{avll}	Address Valid to ALE Low @ 12 MHz @ 16 MHz	 63.3 42.5		 (1+2M) T_{OSC} – 20		ns (3)
T_{llax}	Address Hold after ALE Low @ 12 MHz @ 16 MHz	 10 10		 10		ns
T_{RLRH} (2)	RD# or PSEN# Pulse Width @ 12 MHz @ 16 MHz	 156.6 115		 2(1+N) T_{OSC} – 10		ns (4)
T_{wlwh}	WR# Pulse Width @ 12 MHz @ 16 MHz	 156.6 115		 2(1+N) T_{OSC} – 10		ns (4)
T_{llrl} (2)	ALE Low to RD# or PSEN# Low @ 12 MHz @ 16 MHz	 63.3 42.5		 T_{OSC} – 20		ns
T_{lhax}	ALE High to Address Hold @ 12 MHz @ 16 MHz	 83.3 62.5		 (1+2M) T_{OSC}		ns (3)

NOTES:
1. 16 MHz.
2. Specifications for PSEN# are identical to those for RD#.
3. In the formula, M=Number of wait states (0 or 1) for ALE.
4. In the formula, N=Number of wait states (0,1,2, or 3) for RD#/PSEN#/WR#
5. “Typical” specifications are untested and not guaranteed.

Table 11. AC Characteristics (Capacitive Loading = 50 pF) (Continued)

Symbol	Parameter	@ Max F_{osc} (1)		F_{osc} Variable		Units
		Min	Max	Min	Max	
T_{RLDV} (2)	RD#/PSEN# Low to valid Data/Instruction In @ 12 MHz @ 16 MHz		 116.6 75		 2(1+N) Tosc – 50	ns (4)
T_{RHDX} (2)	Data/Instruction Hold Time. Occurs after RD#/PSEN# are exerted to V_{OH}	0		0		ns
T_{RLAZ} (2)	RD#/PSEN# Low to Address Float	Typ.=0 (5)	2	Typ. = 0 (5)	2	ns
T_{rhdz1}	Instruction Float after RD#/PSEN# High @ 12 MHz @ 16 MHz		 10 10		 10	ns
T_{rhdz2}	Data Float after RD#/PSEN# High @ 12 MHz @ 16 MHz		 176.6 135		 2Tosc +10	ns
T_{rhlh1}	RD#/PSEN# High to ALE High (Instruction) @ 12 MHz @ 16 MHz	 10 10		 10		ns
T_{RHLH2}	RD#/PSEN# High to ALE High (Data) @ 12 MHz @ 16 MHz	 176.6 135		 $2T_{osc}$ + 10		ns
T_{WHLH}	WR# High to ALE High @ 12 MHz @ 16 MHz	 176.6 135		 $2T_{osc}$ + 10		ns
T_{avdv1}	Address (P0) Valid to Valid Data/Instruction In @ 12 MHz @ 16 MHz		 263.2 180		 4(1+M/2) T_{OSC} – 70	ns (3)
T_{avdv2}	Address (P2) Valid to Valid Data/Instruction In @ 12 MHz @ 16 MHz		 278.2 195		 4(1+M/2) T_{OSC} – 55	ns (3)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In @ 12 MHz @ 16 MHz		 116.6 75		 $2T_{OSC}$ – 50	ns

NOTES:
1. 16 MHz.
2. Specifications for PSEN# are identical to those for RD#.
3. In the formula, M=Number of wait states (0 or 1) for ALE.
4. In the formula, N=Number of wait states (0,1,2, or 3) for RD#/PSEN#/WR#
5. “Typical” specifications are untested and not guaranteed.

Table 11. AC Characteristics (Capacitive Loading = 50 pF) (Continued)

Symbol	Parameter	@ Max F_{osc} (1)		F_{osc} Variable		Units
		Min	Max	Min	Max	
T_{avrl} (2)	Address Valid to RD#/PSEN# Low @ 12 MHz @ 16 MHz	 146.6 105		 2(1+M) T_{OSC} – 20		ns (3)
T_{avwl1}	Address (P0) Valid to WR# Low @ 12 MHz @ 16 MHz	 156.6 115		 2(1+M) T_{OSC} – 10		ns (3)
T_{AVWL2}	Address (P2) Valid to WR# Low @ 12 MHz @ 16 MHz	 166.6 125		 2(1+M) T_{OSC}		ns (3)
T_{WHQX}	Data Hold after WR# High @ 12 MHz @ 16 MHz	 63.3 42.5		 T_{OSC} – 20		ns
T_{QVWH}	Data Valid to WR# High @ 12 MHz @ 16 MHz	 143.6 102		 2(1+N) T_{OSC} – 23		ns (4)
T_{WHAX}	WR# High to Address Hold @ 12 MHz @ 16 MHz	 146.6 105		 2T_{OSC} – 20		ns

NOTES:
1. 16 MHz.
2. Specifications for PSEN# are identical to those for RD#.
3. In the formula, M=Number of wait states (0 or 1) for ALE.
4. In the formula, N=Number of wait states (0,1,2, or 3) for RD#/PSEN#/WR#
5. “Typical” specifications are untested and not guaranteed.

SYSTEM BUS TIMINGS

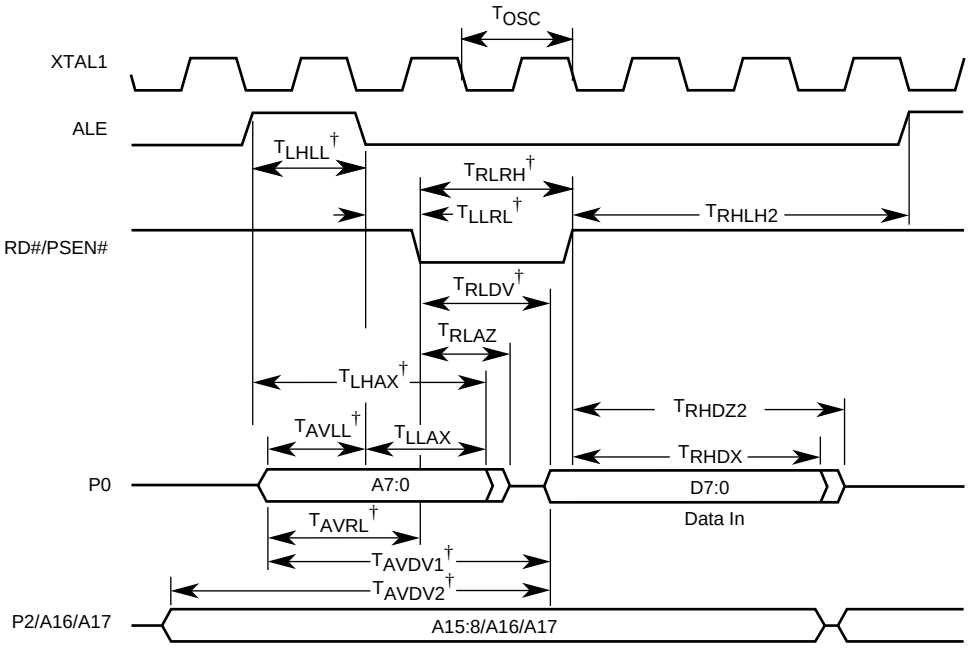
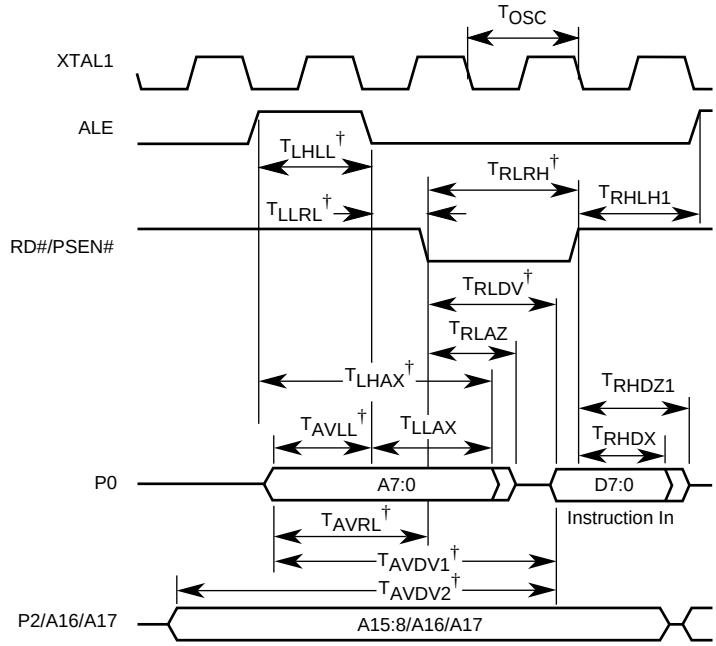


Figure 6. External Read Data Bus Cycle in Nonpage Mode



† The value of this parameter depends on wait states. See the table of AC characteristics.

A4211-01

Figure 7. External Instruction Bus Cycle in Nonpage Mode

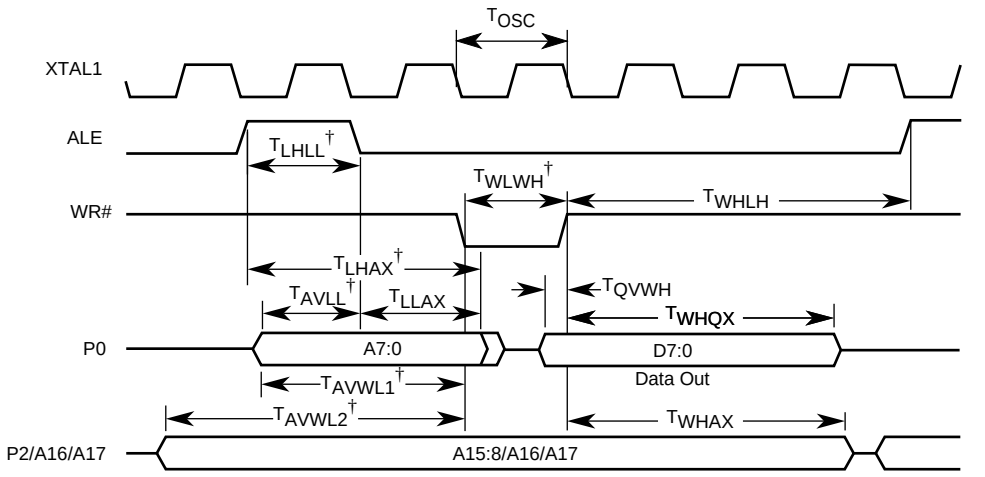


Figure 8. External Write Data Bus Cycle in Nonpage Mode

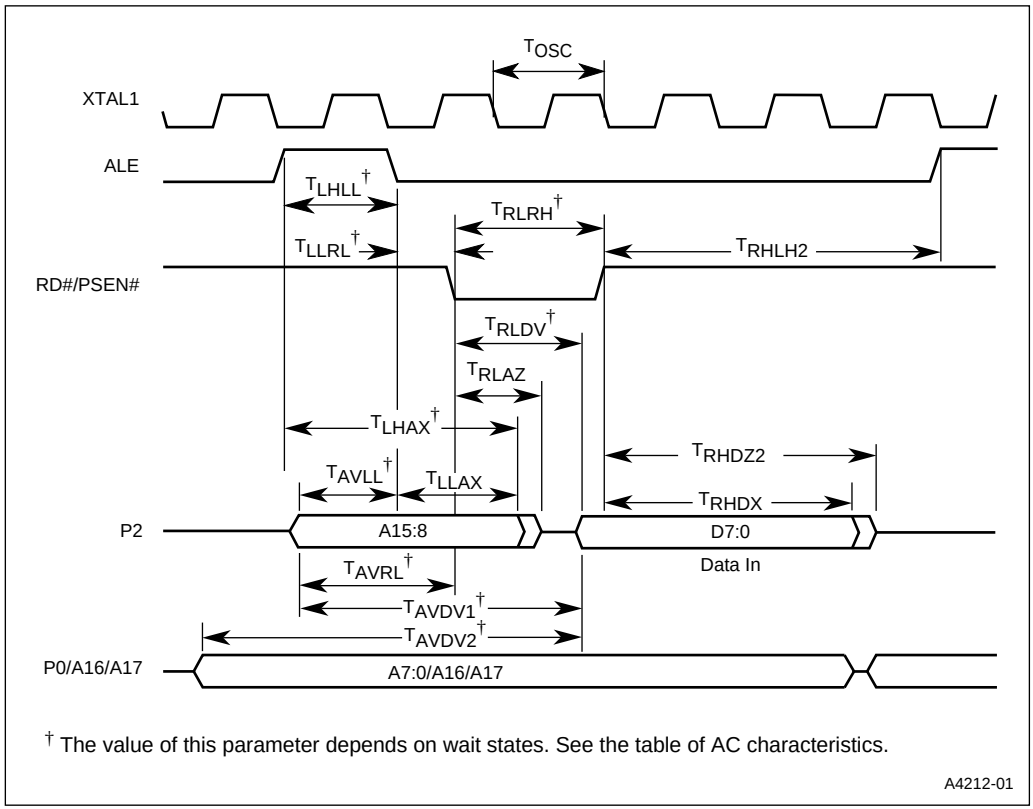
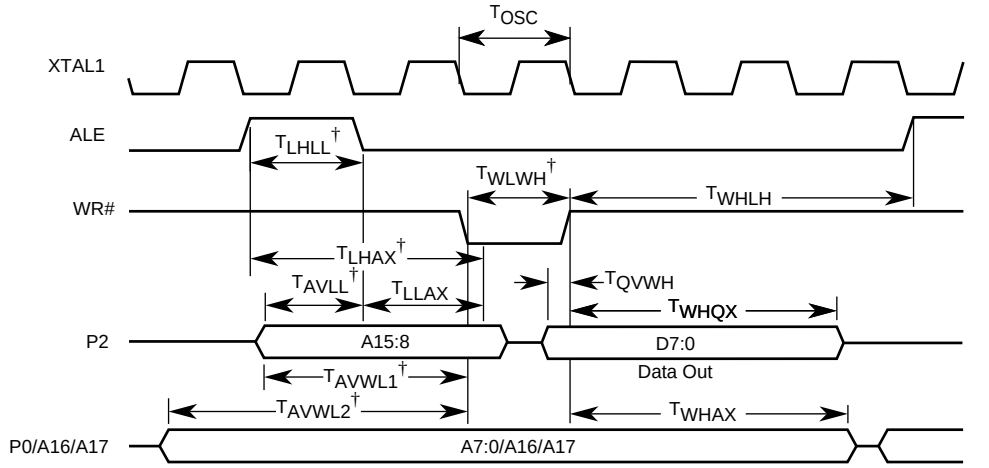


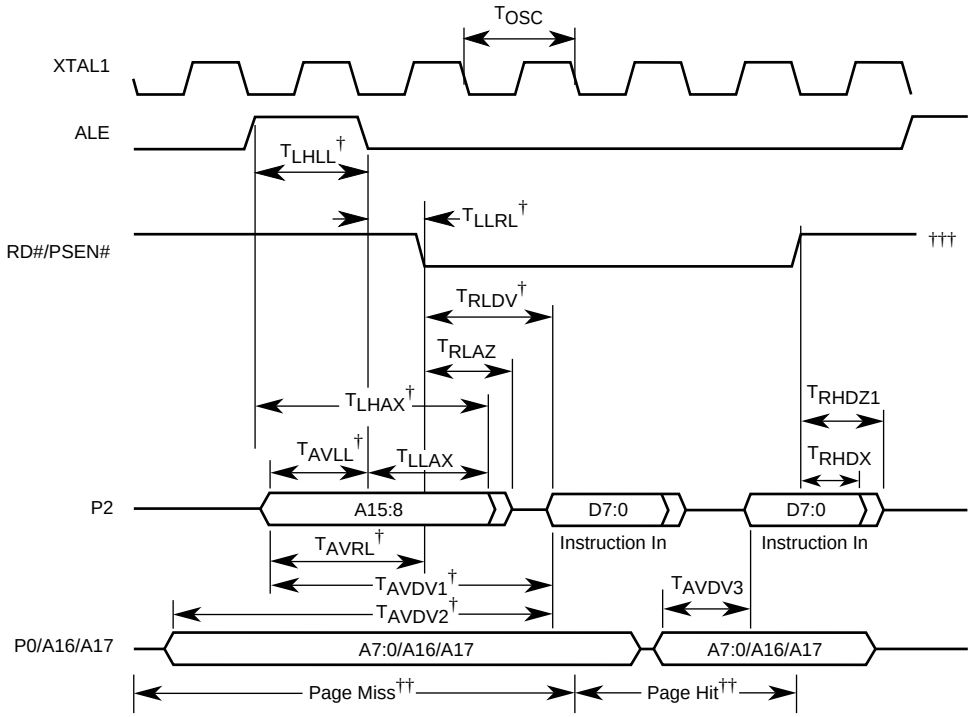
Figure 9. External Read Data Bus Cycle in Page Mode



† The value of this parameter depends on wait states. See the table of AC characteristics.

A4182-01

Figure 10. External Write Data Bus Cycle in Page Mode



† The value of this parameter depends on wait states. See the table of AC characteristics.

†† A page hit (i.e., a code fetch to the same 256-byte "page" as the previous code fetch) requires one state ($2T_{OSC}$); a page miss requires two states ($4T_{OSC}$).

††† During a sequence of page hits, PSEN# remains low until the end of the last page-hit cycle.

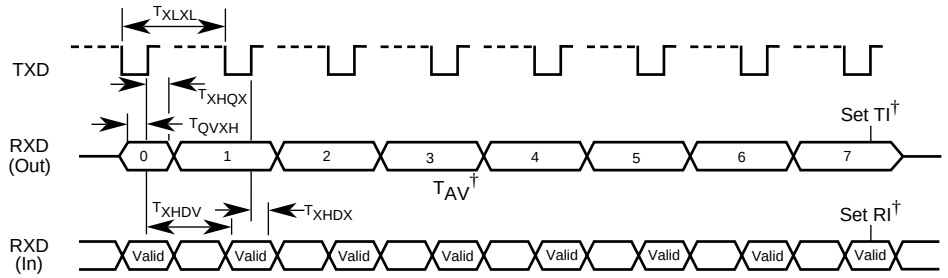
A4213-02

Figure 11. External Instruction Bus Cycle in Page Mode

AC Characteristics — Serial Port, Shift Register Mode

Table 12. Serial Port Timing — Shift Register Mode

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Cycle Time	$12T_{OSC}$		ns
T_{QVSH}	Output Data Setup to Clock Rising Edge	$10T_{OSC} - 133$		ns
T_{XHQX}	Output Data hold after Clock Rising Edge	$2T_{OSC} - 117$		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		$10T_{OSC} - 133$	ns



†TI and RI are set during S1P1 of the peripheral cycle following the shift of the eighth bit.

A2592-02

Figure 12. Serial Port Waveform — Shift Register Mode

External Clock Drive

Table 13. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency (F_{OSC})		16	MHz
T_{CHCX}	High Time	20		ns
T_{CLCX}	Low Time	20		ns
T_{CLCH}	Rise Time		10	ns
T_{CHCL}	Fall Time		10	ns

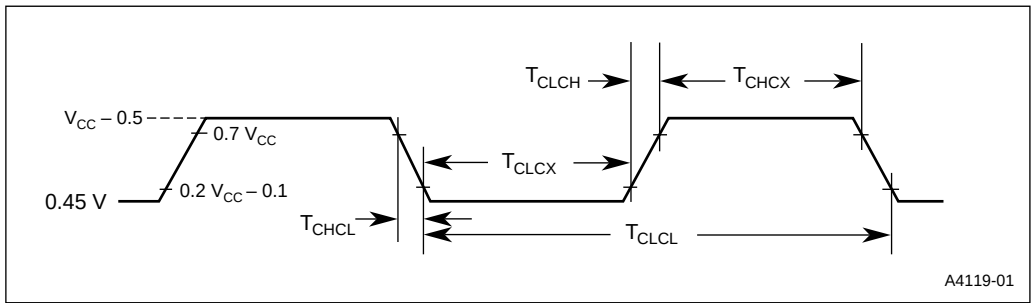


Figure 13. External Clock Drive Waveforms

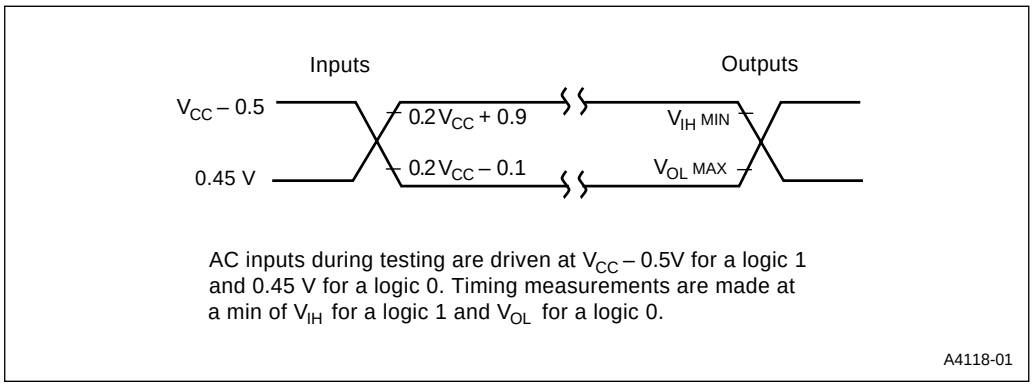
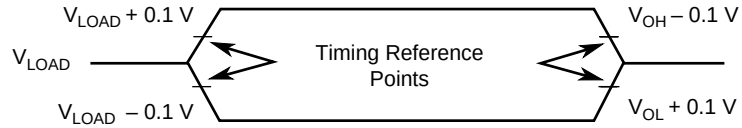


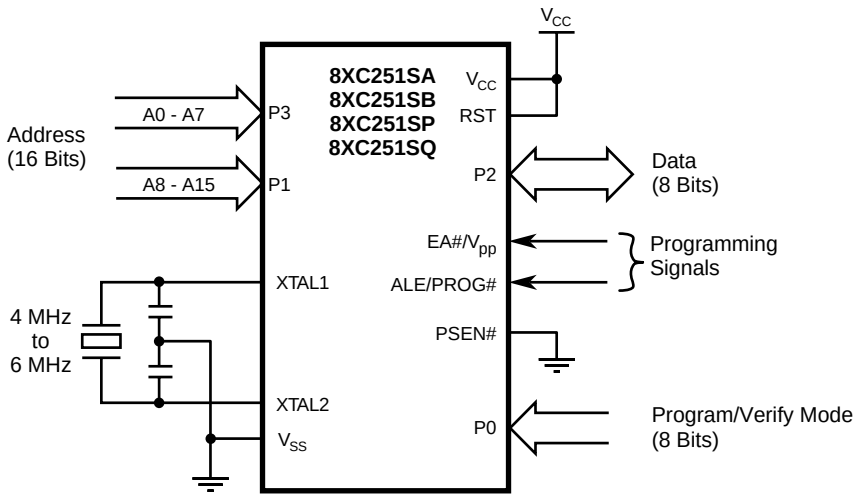
Figure 14. AC Testing Input, Output Waveforms



For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with I_{OL}/I_{OH} = ± 20 mA.

A4117-01

Figure 15. Float Waveforms



A4209-01

Figure 16. Setup for Programming and Verifying Nonvolatile Memory

PROGRAMMING AND VERIFYING NONVOLATILE MEMORY

The 87C251SA/SB/SP/SQ has several areas of nonvolatile memory that can be programmed and/or verified: on-chip code memory (16 Kbytes), lock bits (3 bits), encryption array (128 bytes), and signature bytes (3 bytes). The *8XC251SA/SB/SP/SQ User's Manual* (Order Number: 272795) provides procedures for programming and verifying the nonvolatile memory.

Figure 16 shows the setup for programming and/or verifying the nonvolatile memory. Table 14 lists the programming and verification operations and indicates which operations apply to the different versions of the 87C251SA/SB/SP/SQ. It also specifies the signals on the programming input (PROG#) and the ports. The ROM/OTPROM/EPROM mode (port 0) specifies the operation (program or verify) and the base address of the memory area. The addresses (ports 1 and 3) are relative to the base address. (On-chip memory for an 8-Kbyte ROM/OTPROM/EPROM device is located at address range FF:0000H–FF:1FFFH. On-chip memory for a 16-Kbyte ROM/OTPROM/EPROM device is located at address range FF:0000H–FF:3FFFH. The other areas of the ROM/OTPROM/EPROM are outside the memory address space and are accessible only during programming and verification.)

Information in Figures 17 and 18 define the configuration bits. Figure 19 shows the waveforms for the programming and verification cycles, and Table 15 lists the timing specifications. The signature bytes of the 83C251SA/SB/SP/SQ ROM versions and the 87C251SA/SB/SP/SQ OTP versions are factory programmed. Table 16 lists the addresses and the contents of the signature bytes.

Factory-programmed ROM and OTPROM versions of 8XC251SA/SB/SP/SQ use configuration byte information supplied in a separate hexadecimal disk file. 8XC251SA/SB/SP/SQ devices without internal ROM/OTPROM/EPROM arrays fetch configuration byte information from external application memory based on an internal address range of FF:FFF9:8H.

NOTE:

The V_{PP} source in Figure 16 must be well regulated and free of glitches. The voltage on the V_{PP} pin must not exceed the specified maximum, even under transient conditions.

Table 14. Programming and Verification Modes

Mode	8XC251SA/SB/SP/SQ		PROG#	P0	P2	Addresses P1 (high), P3 (low)	Notes
	X = 7	X = 3					
Program on-chip code memory	Y		5 Pulses	68H	Data	0000H–3FFFH (16K) 000H-1FFFH (8K)	1
Verify on-chip code memory	Y	Y	High	28H	Data	0000H–3FFFH (16K) 0000H-1FFFH (8K)	
Program configuration bytes							2
Verify configuration bytes							2
Program lock bits	Y		25 Pulses	6BH	XX	0001H–0003H	1, 3
Verify lock bits	Y	Y	High	2BH	Data	0000H	4
Program encryption array	Y		25 Pulses	6CH	Data	0000H–007FH	1
Verify signature bytes	Y	Y	High	29H	Data	0030H, 0031H, 0060H	

NOTES:
1. The PROG# pulse waveform is shown in Figure 19.
2. Factory-programmed ROM, OTPROM and EPROM versions of 8XC251SA/SB/SP/SQ use configuration byte information supplied in a separate hexadecimal disk file. 8XC251SA/SB/SP/SQ devices without internal ROM/OTPROM/EPROM arrays fetch configuration byte information from external application memory based on an internal address range of FF:FFF9:8H.
3. When programming the lock bits, the data bits on port 2 are don't care. Identify the lock bits with the address as follows: LB3 - 0003H, LB2 - 0002H, LB1 - 0001H
4. The three lock bits are verified in a single operation. The states of the lock bits appear simultaneously at port 2 as follows: LB3 - P2.3, LB2 - P2.2. LB1 - P2.1. High = programmed.

UCONFIG0 Address FF:FFF8H

7							0
UCON	WSA1#	WSA0#	XALE#	RD1	RD0	PAGE#	SRC

Bit Number	Bit Mnemonic	Function
7	UCON	Configuration byte location selector: Clearing this bit causes the device to fetch configuration information from on-chip memory. Setting this bit causes the device to locate configuration information based upon the state of EA# during reset (EA# = V_{CC} = on-chip; EA# = V_{SS} = off-chip).
6:5	WSA1#, WSA0# (see Note)	Wait State Select (for all pages except 01H). WSA0# is identical to the WSA bit defined in the 8XC251SB A-step: WSA1# WSA0# Description 1 1 No wait states (01: page controlled by CONFIG1) 1 0 Insert 1 wait state for all pages except the 01: page 0 1 Insert 2 wait states for all pages except the 01: page 0 0 Insert 3 wait states for all pages except the 01: page
4	XALE#	Extend Ale: If this bit is set, the time of the ALE pulse is T_{OSC}. Clearing this bit extends the time of the ALE pulse from T_{OSC} to $3T_{OSC}$, which adds one external wait state.
3:2	RD1, RD0	RD# and PSEN# function select: RD1 RD0 RD# Range P1.7/CEX4/A17 PSEN# Range 0 0 RD# = A16 A17 only All Addresses 0 1 RD# = A16 P1.7/CEX4 All Addresses 1 0 P3.7 only P1.7/CEX4 All Addresses 1 1 ≤ 7F:FFFFH P1.7/CEX4 ≥ 80:0000H
1	PAGE#	Page Mode Select: Clear this bit for page-mode (A15:8/D7:0 on P2, and A7:0 on P0). Set this bit for nonpage-mode (A15:8 on P2, and A7:0/D7:0 on P0 (compatible with MCS 51 microcontrollers)).
0	SRC	Source Mode/Binary Mode Select: Set this bit for source mode. Clear this bit for binary mode (binary-code compatible with MCS 51 microcontrollers).

Figure 17. Configuration Byte 0

NOTE:

Factory-programmed ROM, OTPROM and EPROM versions of 8XC251SA/SB/SP/SQ use configuration byte information supplied in a separate hexadecimal disk file. 8XC251SA/SB/SP/SQ devices without internal ROM/OTPROM/EPROM arrays fetch configuration byte information from external application memory based on an internal address range of FF:FFF9:8H.

UCONFIG1 Address FF:FFF9H

7							0
—	—	—	INTR	WSB	WSB1#	WSB0#	EMAP#

Bit Number	Bit Mnemonic	Function
7:5	—	Reserved; set these bits when writing to UCONFIG1.
4	INTR	Interrupt Mode: If this bit is set, interrupts push 4 bytes onto the stack (the 3 bytes of the PC register and the PSW1 register). If this byte is clear, interrupts push 2 bytes onto the stack (the 2 lower bytes of the PC register).
3	WSB	Wait State B. Only use this bit for A-step compatibility: Clear this bit to generate one external wait state for memory region 01:. Set this bit for no wait states for region 01:.
2:1	WSB1#, WSB0#	Wait States (01:XXXXH page only) WSB1# WSB0# Description 11 No wait states 10 Insert 1 wait state for the 01: page 01 Insert 2 wait states for the 01: page 00 Insert 3 wait states for the 01: page
0	EMAP#	EPROM MAP: Clearing this bit maps the upper 8 Kbytes of on-chip code memory (FF:2000H–FF:3FFFH) to 00:E000H–00:FFFFH. If this bit is set, the upper 8 Kbytes of on-chip code memory are mapped only to FF:2000H–FF:3FFFH. If this bit is set mapping does not occur.

Figure 18. Configuration Byte 1

NOTE:

Factory-programmed ROM and OTPROM versions of 8XC251SA/SB/SP/SQ use configuration byte information supplied in a separate hexadecimal disk file. 8XC251SA/SB/SP/SQ devices without internal ROM/OTPROM/EPROM arrays fetch configuration byte information from external application memory based on an internal address range of FF:FFF9:8H.

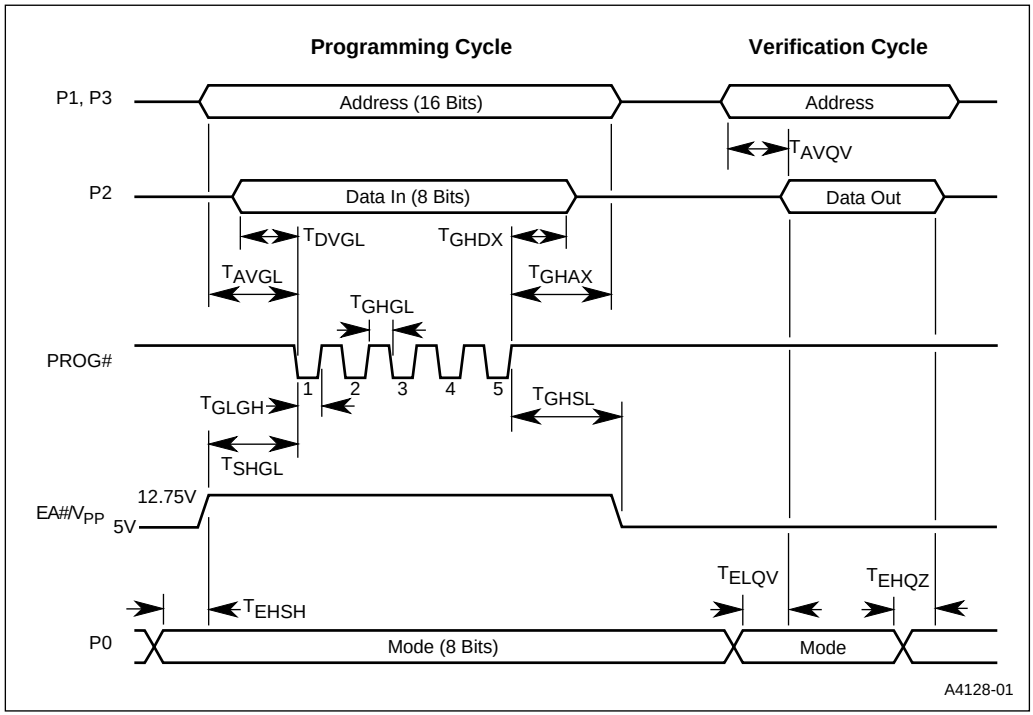


Figure 19. Timing for Programming and Verification of Nonvolatile Memory

Table 15. Nonvolatile Memory Programming and Verification Characteristics at T_A = 21 – 27 °C, V_{CC} = 5 V, and V_{SS} = 0 V

Symbol	Definition	Min	Max	Units
Vpp	Programming Supply Voltage	12.5	13.5	D.C. Volts
Ipp	Programming Supply Current		75	mA
Fosc	Oscillator Frequency	4.0	6.0	MHz
T_{AVGL}	Address Setup to PROG# Low	$48T_{OSC}$		
T_{GHAX}	Address Hold after PROG#	$48T_{OSC}$		
T_{DVGL}	Data Setup to PROG# Low	$48T_{OSC}$		
T_{GHDX}	Data Hold after PROG#	$48T_{OSC}$		
T_{EHSH}	ENABLE High to V_{PP}	$48T_{OSC}$		
T_{SHGL}	V_{PP} Setup to PROG# Low	10		µs
T_{GHSL}	V_{PP} Hold after PROG#	10		µs
T_{GLGH}	PROG# Width	90	110	µs
T_{AVQV}	Address to Data Valid		$48T_{OSC}$	
T_{ELQV}	ENABLE Low to Data Valid		$48T_{OSC}$	
T_{EHQZ}	Data Float after ENABLE	0	$48T_{OSC}$	
T_{GHGL}	PROG# High to PROG# Low	10		µs

NOTE: Notation for timing parameters:

A = Address D = Data E = Enable G = PROG# H = High L = Low

Q = Data out S = Supply (V_{PP}) V = Valid X = No Longer Valid Z = Floating

Table 16. Contents of the Signature Bytes

ADDRESS	CONTENTS	DEVICE TYPE
30H	89H	Indicates Intel Devices
31H	40H	Indicates MCS251 core product
60H	7AH	Indicates 83C251SA device
60H	7BH	Indicates 83C251SB device
60H	4AH	Indicates 83C251SP device
60H	4BH	Indicates 83C251SQ device
60H	FAH	Indicates 87C251SA device
60H	FBH	Indicates 87C251SB device
60H	CAH	Indicates 87C251SP device
60H	CBH	Indicates 87C251SQ device
61H	55H	Indicates 8XC251SA/SB/SP/SQ B-step products

Revision History

The following changes appear in the -004 datasheet:

1. To address the fact that many of the package prefix variables have changed, all package prefix variables in the document are now indicated with an "**x**".

The (-003) revision of the 8XC251SA/SB/SP/SQ datasheet contains information on products with “[M] [C] '94 '95 C” as the last line of the topside marking. This datasheet replaces earlier product information. The following changes appear in the -003 datasheet:

1. UCONFIG0.7 (UCON) is now defined.
2. Real time wait state operation is described in the datasheet.
3. Memory map reserved locations are newly defined.

The (-002) revision of the 8XC251SA/SB/SP/SQ datasheet contains information on products with “[M] [C] '94 '95 B” as the last line of the topside marking. This datasheet replaces earlier product information. The following changes appear in the -002 datasheet:

1. A corrected PDIP diagram appears on page 7.
2. A corrected formula to calculate T_{LHLL} is described on page 17.
3. The RD#/PSEN# waveform is changed in Figure 11 on page 25.